

IN THE CLAIMS:

1. (Currently Amended) A process for transmission of a message in a system, said process comprising the steps of sending, receiving, or propagating 1) more than one packet and 2) an Interpacket gap, said packet comprising a start-of-stream delimiter, and a series of at least 16 message bytes encoded in symbols uninterrupted by a control symbol, and said Interpacket gap comprising a plurality of symbols decoded as Idle symbols wherein said Interpacket gap includes at least one non-Idle symbol such that the presence of said non-Idle symbol is part of a message, wherein an Idle symbol is defined according to a packet transmission standard.

2. (Original) The process of claim 1 wherein said system comprises Fast Ethernet.

3. (Original) The process of claim 2 wherein said non-Idle symbol in said interpacket gap is the symbol for zero.

4. (Original) The process of claim 2 wherein said non-Idle symbol is a symbol having only one zero bit.

5. (Original) The process of claim 1 wherein said system comprises Gigabit Ethernet.

6. (Original) The process of claim 5 wherein said non-Idle symbol comprises a K28.5/Dxx.y or K28.1/Dxx.y sequence.

7. (Original) The process of claim 1 wherein said message comprises a side-channel.

8. (Currently Amended) A process for transmission of messages in a system, said process comprising the steps of sending, receiving, or propagating 1) more than one packet and 2) an interpacket gap, said packet comprising an information-carrying portion between a start-of-packet delimiter and an end-of-packet delimiter, said information-carrying portion including a start-of-

~~stream delimiter, and a series of at least 16 information bytes encoded in standard symbols and at least one non-standard symbol, wherein said standard symbols are defined according to a packet transmission standard uninterrupted by a control symbol wherein said packet includes a plurality of non-standard symbols as part of a message~~

9. (Original) The process of claim 8 wherein said interpacket gap includes both at least one symbol decoded as an Idle symbol and at least one non-Idle symbol such that the presence of said non-Idle symbol is part of a message.

10. (Original) The process of claim 9 wherein said system compromises Fast Ethernet.

11. (Original) The process of claim 10 wherein said non-Idle symbol is the symbol for zero.

12. (Original) The process of claim 10 wherein said non-Idle symbol is a symbol having only one zero bit.

13. (Original) The process of claim 9 wherein said system comprises Gigabit Ethernet.

14. (Original) The process of claim 13 wherein said non-Idle symbol comprises a K28.5/Dxx.y or K28.1/Dxx.y sequence.

Claims 15-20 (Canceled)

21. (Currently Amended) An apparatus, comprising:
a transmitter configured to transmit a signal having a plurality of packets and an interpacket gap, said interpacket gap having symbols decoded as an Idle symbol, said Idle symbol defined according to an Ethernet standard, said transmitter including:

a buffer configured to store a message to be inserted into said interpacket gap;

a formatter configured to modify a bit stream representing said message to allow identification of message boundaries and to allow establishment of word alignment within said bit stream; and

an encoder configured to substitute at least one message symbol for one of said symbols decoded as an Idle symbol in said interpacket gap to encode at least a portion of said message into said interpacket gap, wherein said at least one message symbol is decoded as an Idle symbol according to said Ethernet standard.

22. (Previously Presented) The apparatus of claim 21 wherein said formatter is configured to modify said bit stream with an HDLC flag.

23. (Previously Presented) The apparatus of claim 22 wherein said formatter is configured to insert a logic zero to said bit stream to avoid recognition of a portion of said message as said flag.

24. (Currently Amended) The apparatus of claim 21 wherein said Ethernet standard is Institute of Electrical and Electronic Engineers (IEEE) Standard 802.3 ~~signal comprises an Ethernet~~ signal.

25. (Previously Presented) The apparatus of claim 21 wherein said at least one message symbol substituted by said encoder represents a logic 1.

26. (Previously Presented) The apparatus of claim 21 wherein said at least one message symbol substituted by said encoder represents a logic 0.